



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/574,745

05/18/2000

Charles Barry

M-8875 US

9947

7590

02/08/2005

Sawyer Law Group  
2465 E. Bayshore Road  
Suite 406  
Palo Alto, CA 94303

EXAMINER

LY, ANH VU H

ART UNIT

PAPER NUMBER

2667

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/574,745

Applicant(s)

BARRY ET AL.

Examiner

Anh-Vu H Ly

Art Unit

2667

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 3-15 and 22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13 and 14 is/are allowed.
- 6) ☒ Claim(s) 3-12 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Response to Amendment***

1. This communication is in response to applicant's amendment filed June 21, 2004. The proposed amendment to the claims has been entered. Claims 3-15 and 22 are pending.

***Claim Objections***

2. Claims 12-14 and 22 are objected to because of the following informalities:

With respect to claim 12, in line 3, "said master clock signal" lacks antecedent basis.

With respect to claims 13-14 and 22, in line 6, "said one of said nodes" lacks clear antecedent basis.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 3, 8, 9, 11, and 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (US Patent 6,438,175) in view of Hamano et al (US Patent 5,610,660).

With respect to claims 3 and 22, Yamashita discloses (col. 13, lines 29-44 and Fig. 4) a method for synchronizing nodes by generating a control signal during a transmission of a data frame, comprising steps of receiving the serial data DZS, the S/P converting and clock detecting unit 21 reproduced the DZ(10) signal. Then, the synchronous word data detector 24 reproduced a synchronous SKD signal (receiving, by second node, the control signal after receiving only a

Art Unit: 2667

portion of the data frame). Then supplying the SKD signal to the word clock generator 22 and the synchronous signal forming unit 25 to reproduce local clocks and receive data (performing, by second node, an action required by the control signal prior to waiting until the data frame has been fully received). Yamashita does not disclose that wherein the control signal was inserted in the data frame outside of a payload field of the data frame. Hamano discloses (see Abstract) the synchronous word is inserted to each header of the slices. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the feature of inserting the synchronous word into the header in Yamashita's system, as suggested by Hamano, therefore, the payload section only carries the information data.

With respect to claim 8, Yamashita discloses in Fig. 5, that the control signal is an 8B/10B encoded control characters, namely +K(28.5) and D(21.5) (the control signal is an 8B/10B encoded control character).

With respect to claim 9, Yamashita discloses in Fig. 6, the concept of a data frame used in transmitting digital data (wherein data frame is a packet).

With respect to claim 11, Yamashita discloses in Fig. 4, a block diagram illustrating a data receiving apparatus for receiving data transmitted from the data transmission apparatus (performing an action by MAC).

Art Unit: 2667

4. Claims 4, 10, 12, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (US Patent 6,438,175) and Hamano et al (US Patent 5,610,660) further in view of Brede et al (US Patent 5,726,607).

With respect to claims 4, 10, 12, 15, and 22, Yamashita and Hamano have addressed all of the limitations recited in independent claim 3. Yamashita does not disclose generating local clock signals by a local clock in the second node; correcting any timing error action in the local clock so that the timing jitter is limited to less than a data frame period (or MAC layer encoded character); wherein, the control signal is a master clock signal; performing an action to correct a timing error between a local clock and the master clock; and performing an action to synchronize the local clock with the control signal. Brede discloses (Col. 3, lines 43-45 and Fig. 1) a micro-controller based phase lock loop that locks onto a 1.544 MHz primary timing reference signal and produces a jitter free local 2.56 MHz phase aligned system output clock. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the features of generating a local clock signal from the master control clock signal provided by the remote node so that any timing jitter between the master control clock signal and the local clock signal is limited to less than a data frame period or even free in Yamashita's system, as suggested by Brede, to prevent corrupting the received data.

5. Claims 5 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (US Patent 6,438,175) and Hamano et al (US Patent 5,610,660) and Brede (US Patent 5,726,607) further in view of Ofek (US Patent 6,259,695).

With respect to claims 5 and 6, Yamashita and Hamano have addressed all of the limitations recited in independent claim 3. Yamashita does not disclose that the master clock signal is an 8 KHz clock and the 8 KHz is a GPS clock. Ofek discloses (col. 9, lines 30-31 and Fig. 1) a method of distributing common timing reference to both packet and telephony switch networks. The method comprises a GPS receiver 20 receives timing references from satellites and distributes a common time reference, CTR, and 8 KHz reference clock, to the remote network nodes via output ports. Therefore, it would have been obvious to one having ordinary skill in the art, at the time of invention, to utilize globally available GPS and an 8 KHz as the master clock signals, for couple of key motivations. Firstly, the GPS is globally available providing highly accurate timing reference at a very affordable cost as taught by Ofek (col. 3, lines 52-53 and lines 60-61). Secondly, it is common practice and is widely deployed in the telephony switch networks to synchronize networking equipments with an 8 KHz clock master signal.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (US Patent 6,438,175) and Hamano et al (US Patent 5,610,660).

With respect to claim 7, Yamashita and Hamano have addressed all of the limitations recited in independent claim 3. Yamashita does not disclose that the data frame is transmitted in accordance with an Ethernet protocol. However, Ethernet protocol is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to transmit data according to Ethernet protocol in Yamashita's system, to be compatible with other Ethernet networks.

***Allowable Subject Matter***

7. Claims 13-14 are allowed.

***Response to Arguments***

8. Applicant's arguments with respect to claims 3-15 and 22 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H Ly whose telephone number is 571-272-3175. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

Art Unit: 2667

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

avl

  
CHI PHAM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2667 2/4/05